# METHOD AND APPARATUS FOR IMPLEMENTING POWER CONTROL IN MULTI-VOLTAGE I/O CIRCUITS

## Field of the Invention

The present invention relates generally to the data processing field, and more particularly, relates to a method and apparatus for implementing power control in multi-voltage input/output (I/O) circuits.

## Description of the Related Art

As technologies evolve, power supply voltages are being reduced and I/O performance requirements are increasing. In addition, I/O circuits are often required to support more than one generation of technologies and this requires the I/O circuits to operate over an increasing range of power supply voltages.

High performance differential receivers in these I/O circuits generally require a DC bias current. This DC bias current can result in excessive power dissipation when circuits are designed to meet performance at lower voltages and then are operated at higher voltages. Regulators or dropping resistors are either expensive or performance limiting.

A need exists for a mechanism for implementing power control in multi-voltage input/output (I/O) circuits. It is desirable to provide such a mechanism for implementing power control in multi-voltage input/output (I/O) circuits that is simple to implement and generally effective without limiting performance.

## Summary of the Invention

Principal aspects of the present invention are to provide a method and apparatus for implementing power control in multi-voltage input/output (I/O) circuits. Other important aspects of the present invention are to provide such method and apparatus for implementing power control in multi-voltage input/output (I/O) circuits substantially without negative effect and that overcome many of the disadvantages of prior art arrangements.

In brief, a method and apparatus are provided for implementing power control in multi-voltage input/output (I/O) circuits. First current biasing devices are provided for creating a first constant bias current. Second current biasing devices are provided for creating a second bias current. The second current biasing devices are activated at a first voltage and are deactivated at a second voltage. The first voltage is less than the second voltage.

In accordance with features of the invention, apparatus for implementing power control in multi-voltage input/output (I/O) circuits includes a first set of current biasing devices and a second set of current biasing devices. The first set of current biasing devices is always on and the second set of current biasing devices is only activated to create a second bias current at a lower power supply voltage to maintain performance.

In accordance with features of the invention, each of the first set of current biasing devices and the second set of current biasing devices include a plurality of field effect transistors that are arranged in parallel. A gate input to the second set of current biasing field effect transistors (FETs) activates the FETs at the lower power supply voltage and deactivates the FETs at a higher power supply voltage.

## Brief Description of the Drawings

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings, wherein:

FIGS. 1 and 2 together provide a schematic diagram of an exemplary I/O circuit for implementing power control for multi-voltage applications in accordance with the preferred embodiment; and

FIG. 3 is a schematic diagram of an exemplary bias control generating circuit for use with the I/O circuit of FIGS. 1 and 2 in accordance with the preferred embodiment.

**Detailed Description of the Preferred Embodiments**

In accordance with features of the invention, a first set of current biasing devices is constantly activated, and a second set of current biasing devices is activated at lower voltage applications to maintain a desired current.

Having reference now to the drawings, in FIGS. 1 and 2 there is shown an exemplary I/O circuit for implementing power control for multi-voltage applications in accordance with the preferred embodiment generally designated by the reference character 100. I/O circuit 100 can be operated at a selected or variable voltage rail labeled VDD, for example, at 2.5 volts or 1.8 volts.

Referring now to FIG. 1, I/O circuit 100 includes a first pair of P-channel field effect transistors (PFETs) 102, 104, and a parallel second pair of P-channel field effect transistors (PFETs) 106, 108, each having a source connected to the variable voltage rail VDD. A pair of resistors 109, 110 is connected in series between differential outputs OUTN, OUTP of the I/O circuit 100. Resistors 109, 110 are equal value devices forming a voltage divider to provide a control BIAS signal. A constant gate bias input BIAS is applied to a gate of PFETS 104, 106 that are always on. A selectively enabled gate bias input BIASP2 is applied to a gate of PFETs 102, 108.

I/O circuit 100 includes a differential stage formed by a plurality of N-channel field effect transistors (NFETs) 112, 114, 116, 118. A respective gate input PADR, PADRN is applied to a gate of NFETs 112, 114. The constant gate bias input BIAS is applied to a gate of NFET 116 that is always on. A selectively enabled gate bias input BIASN2 is applied to a gate

of NFET 118. I/O circuit 100 includes a pair of P-channel field effect transistors (PFETs) 120, 122. PFET 120 is connected between a common drain connection of PFETs 102, 104 and the output OUTN. PFET 122 is connected between a common drain connection of PFETs 106, 108 and the output OUTP.

Referring also to FIG. 2, I/O circuit 100 includes a pair of N-channel field effect transistors (NFETs) 130, 132. NFET 130 is connected between the output OUTN and a common drain connection of a pair of NFETs 134, 136. NFET 132 is connected between the output OUTP and a common drain connection of a parallel second pair of NFETs 138, 140. The constant gate bias input BIAS is applied to a respective gate of NFETs 136, 138. The selectively enabled gate bias input BIASN2 is applied to a respective gate of NFETs 134, 140.

Devices PFETs 104, 106, NFET 116 of FIG. 1 and NFETs 136, 138, and PFET 144 of FIG. 2 of the I/O circuit 100 are the basic current biasing devices. PFETs 104, 106, NFET 116 of FIG. 1 and NFETs 136, 138, and PFET 144 of FIG. 2 of the I/O circuit 100 are always on and are controlled by the constant gate bias input signal BIAS.

When the power supply voltage is reduced, BIASP2 and BIASN2 are connected to BIAS creating additional bias current to maintain performance. The second set of current biasing devices including PFETs 102, 108, NFET 118 of FIG. 1 and NFETs 134, 140, and PFET 146 of FIG. 2 of the I/O circuit 100 are turned on by BIASP2 and BIASN2 being connected to BIAS. An exemplary bias control generating circuit for connecting BIASP2 and BIASN2 to BIAS when the power supply voltage is reduced is illustrated and described with respect to FIG. 3. A ratio of the first set or basic current biasing devices and the second set of current biasing devices can be set to maintain constant current for two power supplies.

Referring also to FIG. 3, there is shown an exemplary bias control generating circuit generally designated by the reference character 300 for use with the I/O circuit 100 in accordance with the preferred embodiment.

In accordance with features of the preferred embodiment, BIASP2

and BIASN2 are connected to BIAS by the bias control generating circuit 300 when the power supply voltage is reduced to the lower voltage or 1.8V. When the power supply voltage is increased to the higher voltage or 2.5 V, then BIASP2 and BIASN2 are disabled by the bias control generating circuit 300.

Bias control generating circuit 300 includes a pair of PFETs 160, 162 and an NFET 164. A source of PFET 160 is connected to the voltage supply rail of 2.5 V or 1.8V. A common drain connection of PFET 160 and NFET 164 is provided at node BIASP2. A source of PFET 162 is connected to the common drain connection of PFET 160 and NFET 164 at node BIASP2. A source of NFET 164 and a drain of PFET 162 are connected to BIAS. A gate input CONTROLP is applied to a gate of PFET 160 and NFET 164. A gate input CONTROLN is applied to a gate of NFET 162.

PFETs 160, 162 and NFET 164 are arranged for generating BIASP2 connected to BIAS when the power supply voltage is reduced to the lower voltage or 1.8V.

Bias control generating circuit 300 includes a pair of NFETs 170, 172 and a PFET 174 for selectively connecting BIASN2 to BIAS when the power supply voltage is reduced to the lower voltage or 1.8V. A source of PFET 174 and a drain of NFET 170 are connected to BIAS. A drain of PFET 174 and a source of NFET 170 are connected together at node BIASN2 and are connected to a drain of NFET 172. The source of NFET 172 is connected to ground potential. A gate input CONTROLN is applied to a gate of PFET 174 and NFET 172. A gate input CONTROLP is applied to a gate of NFET 170.

NFETs 170, 172 and PFET 174 are arranged for generating BIASN2 connected to BIAS when the power supply voltage is reduced to the lower voltage or 1.8V.

It should be understood that the present invention is not limited to the illustrated arrangement. For example, it should be understood that the present invention could be extended for more than two power supply values by adding additional parallel devices.

While the present invention has been described with reference to the details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.